

KRISHNA GORAI

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M.Tech (VLSI) · Indian Institute of Technology Mandi · B.Tech (ECE) · NIT Jamshedpur

RTL Design Engineer specializing in **PPA-optimized RTL** and **SoC microarchitecture**. Proficient in **Verilog**, **Computer Architecture**, **low-power design**, and **ASIC Design**.

EDUCATION

Degree	Institute / Board	CGPA / %	Year
M.Tech – VLSI Design	Indian Institute of Technology Mandi	9.03	2025–2027
B.Tech – Electronics and Communication Engineering (ECE)	National Institute of Technology Jamshedpur	8.11	2021–2025
Senior Secondary (Class XII)	CBSE Board	95.2%	2020
Secondary (Class X)	CBSE Board	92.4%	2018

EXPERIENCE

- **Research Intern** | *National Institute of Technology Jamshedpur* Jan 2025 – May 2025
Advisor: Dr. Kunal Singh, Assistant Professor, Electronics and Communication Engineering Dept. Jamshedpur, Jharkhand
Project: Exact Snoop Filter for Multi-Core RISC-V
- Reproduced a published **snoop-coherent cache extension** (SOCC 2024) as a **4-core CV32E40P** sub-system on **Zynq UltraScale+ ZCU104** : per-core write-through L1 D-cache (2 KiB, 2-way, 16 B lines), **AXI4 crossbar**, and a snoop bus with round-robin invalidation and link-register arbiters; cores unmodified. Post-route **60 MHz** timing closed, and the routed netlist verified against RTL.
 - Measured that **38–47%** of cache busy time on matmul/conv2d is spent waiting on the coherence bus, and that **none** of the invalidations delivered in these kernels is necessary. Proposed an **exact snoop filter** (per-core tag-mirror + fill-in-flight tracking) that suppresses invalidations with no sharer and frees the arbiter early: **up to 1.22×** faster on 64^2 matmul for **+1,064 LUT / +516 FF** (<4% of the system).

ACADEMIC PROJECTS

- **SIMTiX — Eight-Lane SIMT Accelerator for RISC-V with Pipelined FP32/FP16 Datapath** Aug 2026
Mtech Project *Paper submitted to VLSID 2027*
- Designed an **8-lane, 4-warp SIMT accelerator** with the full mechanism set — warp scheduling, memory **coalescing**, a per-warp **reconvergence stack**, and a scratchpad — integrated with a 5-stage RISC-V host as a self-contained SoC; re-expressed vector register files and scratchpad as **distributed-RAM (LUTRAM)** banks, cutting LUTs **5.7×** (170.9k → 30.1k) by eliminating the 128-to-1 read multiplexer that otherwise dominates area.
 - Ran a **placed post-route timing-closure study** on Zynq UltraScale+ : diagnosed the FP datapath as **interconnect-bound** at the FMA cone via an explicit delay model, then closed the gap with a **3-stage FMA** and a split fetch/register-read/execute issue engine — raising the swept placed median from **134.0** to **146.4 MHz** (**1.09×**) while cutting the area-time product **46%**.
 - Signed off **at 103.7 MHz** on ZCU104 with a clean DRC (71,567 LUTs, 40 DSPs, 1.20 W); benchmarked **11 kernels** against a scalar RV32I baseline (up to **9.67×** speedup) and measured **22.5%** lane-datapath dynamic energy savings from divergence-aware per-lane clock gating.
- **5-Stage Pipelined RISC-V Processor (RV32I)** 2025
B.Tech Project *Verilog · Python · Vivado*
- Designed a synthesizable **5-stage pipelined RV32I** core (IF/ID/EX/MEM/WB, all 37 base instructions) with a full **forwarding unit**, **load-use stall** detection, branch/jump **flush**, and write-first register-file bypass — **zero inferred latches**, all synchronous-reset.
 - Verified end-to-end in **Vivado 2025.1** (behavioral + **post-implementation functional simulation** on the routed netlist); **timing met @ 83.33 MHz** using **1727 LUTs / 1529 FFs** on Artix-7 XC7A200T.
- **Asynchronous FIFO Design** Jul 2026
Personal Project *Verilog · Vivado*
- Designed a dual-clock Asynchronous FIFO for reliable data transfer between independent clock domains using Verilog HDL.
 - Wrote the **CDC timing constraints** and ran the design through **place and route** on **ZCU104**
- **Low-Power NTT/INTT Accelerator — Configurable Polynomial Compute Engine** Apr 2026
Academic Project | IIT Mandi *Verilog · Xilinx Vivado · Cadence Genus · Cadence Innovus*
- Designed a standalone **configurable compute accelerator** in Verilog supporting 6 operating modes ($n \in \{256, 512, 1024\}$, $q \in \{7681, 12289\}$) with Cooley-Tukey butterfly, Montgomery and Barrett reduction, **clock gating**, and **operand isolation** — achieving **area-power-performance trade-offs** across all modes.
 - Prototyped on **Xilinx Artix-7: 942 LUTs, 574 FFs, 25 DSPs**; **≤142 mW** at 20 MHz; **2066 cycles** per $n=256$ transform; bit-exact outputs validated against cycle-accurate **Python reference model** — all 6 configurations **PASSED**.
 - Taped out on **UMC 130 nm** via Cadence Genus + Innovus (full RTL-to-GDSII): timing closure at **25 MHz** (**WNS +6 ps**, SS corner, 1.08 V, 125°C); **17.65 mW** post-route power; **zero DRC violations**.

- **Snooping and Directory-Based Cache Coherence Protocols for Scalable Multicore Architectures** June 2025
Independent Research Study
 - Conducted a comparative analysis of snooping-based (MSI, MESI, MOESI, Dragon) and directory-based cache coherence protocols, evaluating each along coherence traffic overhead, scalability with core count, and area/complexity trade-offs.
 - Characterized the crossover point beyond which directory-based schemes outperform bus snooping at scale, and analyzed how memory consistency model choice (sequential vs. relaxed) interacts with coherence protocol design decisions.
- **Transistor-Level Digital Design — Circuit Implementation on Cadence Virtuoso** 2024 – 2025
Independent / Academic Mini Projects
 - Implemented and characterized static CMOS gates, Fast Adder circuits, Multipliers, Pseudo-NMOS, dynamic logic, D/SR/JK flip-flops, C²MOS flip-flops, TSPCR and pulse-triggered registers at transistor level; extracted propagation delay, power dissipation, and charge-sharing effects.

TECHNICAL SKILLS

- **RTL Design (Core Skill):** Verilog, Design for Synthesis, FSM Design, FIFO Design, Clock Domain Crossing (CDC), Metastability Analysis, Custom ISA Design
- **Performance / Power / Area (PPA) Optimization:** Pipelining, Re-Timing, Resource Sharing, Clock Gating, Operand Isolation, Dynamic Power Reduction, Performance-Power-Area Trade-off Analysis, Timing and Power Implications of Logic Design
- **Static Timing Analysis (STA):** Setup and Hold Time Analysis, Critical Path Analysis, Timing Closure, Clocking Schemes
- **SoC / ASIC Design Flow:** RTL-to-GDSII Flow, Logic Synthesis, FPGA Implementation, FPGA Prototyping, SoC Design and Integration, Physical Design (Floorplanning, Placement, CTS, Routing, DRC, LVS, GDSII Export)
- **Programming and Scripting:** C/C++, Tcl, Linux
- **EDA / CAD Tools:** Xilinx Vivado, Cadence Genus, Cadence Innovus, Cadence Virtuoso, OpenSTA, GTKWave, Verilator
- **Computer Architecture:** RISC-V, Cache Memory, Cache Optimization Techniques, Processor Micro-architecture
- **Hardware Platforms:** Xilinx Artix-7, Zynq UltraScale+ MPSoC, Xilinx Spartan-3E

KEY COURSES

M.Tech, IIT Mandi: Low Power VLSI Design • Digital Integrated Circuit (IC) Design • CMOS Analog IC Design • Microelectronic Devices and Modeling • Digital VLSI Architectures

B.Tech, NIT Jamshedpur: Analog Electronics • Digital Electronics • Circuit Theory • Digital Signal Processing (DSP)

POSITIONS OF RESPONSIBILITY

- **Teaching Assistant**, School of Computing and Electrical Engineering, IIT Mandi Aug 2025 – Present
– Conducting laboratory sessions and coursework evaluation for Computer Architecture Lab; mentoring students in **Verilog** RTL coding and FPGA-based verification.
- **Event Coordinator**, OJASS 2024 — Annual Techno-Management Fest, NIT Jamshedpur Jan 2024 – May 2024
- **Event Coordinator**, URJA 2024 — Annual Sports Meet, NIT Jamshedpur Aug 2024 – Nov 2024

ACHIEVEMENTS

- **Qualified GATE EC** conducted by IIT Roorkee 2025
- **Qualified JEE Mains** conducted by National Testing Agency (NTA) 2021
- **Qualified JEE Advanced** conducted by IIT Kharagpur 2021