

OM MAHESHWARI

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SUMMARY

Computer architecture and VLSI undergraduate specializing in RISC-V custom ISA extension design, microarchitecture and memory-subsystem simulation (gem5, Spike, QEMU), RTL design, ASIC synthesis, and FPGA prototyping. Four peer-reviewed IEEE publications, one granted patent, and three patent applications spanning ISA design, cache management, and low-power architecture.

EDUCATION

Indian Institute of Technology Mandi (IIT Mandi) <i>B.Tech, Microelectronics and VLSI</i> CGPA: 8.76/10 (as of June 2026)	2023 – 2027
RWTH Aachen University, Germany <i>Semester Exchange</i>	March 2026 – September 2026

EXPERIENCE

Yonsei University - RAISE Lab <i>Research Collaboration - RISC-V Vector Architecture</i>	July 2026 – September 2026 <i>Remote</i>
- Collaborating with the RAISE Lab RISC-V team on vlcap, a supervisor-managed CSR enabling lossless vector-task migration across heterogeneous RISC-V cores with different VLENs. - Jointly developing and validating cross-VLEN architectural-state preservation mechanisms to prevent silent vector-register corruption during OS-level task migration.	
ClimMaTech <i>Co-Founder and CTO</i>	August 2024 – July 2026
- Led end-to-end technical development from concept to deployed product, owning system architecture, edge-AI firmware, and hardware prototyping across the full build cycle. - Developing hybrid, edge-AI sensing nodes that estimate river flow and discharge in real time using optical flow and embedded computer vision, eliminating the need for costly traditional infrastructure.	
Indian Institute of Technology Mandi <i>Research Intern — Bio-Inspired Adaptive Dynamic Precision Scaling for IEEE 754 FPUs</i>	June 2025 – July 2025
- Designed adaptive precision-scaling microarchitecture for IEEE-754 floating-point units (FPUs), modeling accuracy–energy trade-offs at the microarchitectural level. - Implemented dynamic precision control logic in Verilog RTL and evaluated power–accuracy curves across benchmark workloads.	

PROJECTS

Vector-Width Virtualization for RISC-V (vlcap CSR) GitHub	Mar 2026 – Present
- Identified and fixed silent cross-VLEN vector register corruption during OS task migration on heterogeneous RISC-V vector (RVV) systems via a new vlcap CSR, with a formal losslessness proof (Lemma 1). - Implemented and validated across Spike, QEMU, gem5 (SE and dynamic), and a Linux kernel patch series; manuscript under submission in DATE 2027.	
RV-DCX: RISC-V Data Compression Extension <i>Patent filed</i> GitHub	Jan 2026 – Mar 2026
- Designed a custom RISC-V ISA extension accelerating LZ4/Zstd compression by offloading hashing, match-length counting, and bit-field packing into three dedicated execution units (Hash, MLEN, BPACK) integrated into a CVA6-class in-order pipeline; Verilog RTL, synthesized with Yosys. - Achieved 39% (LZ4) and 12% (Zstd) instruction-count reduction and $1.37\times/1.13\times$ speedups (gem5 MinorCPU); multiplier sharing with the M-extension cuts area overhead to $\sim 4.2\%$ ($\sim 6.3\text{K}$ NAND2-eq, 28nm est.), up to $32\times$ performance-per-area for LZ4.	
XSC: Correlation-Aware Stochastic Computing Extension for RISC-V GitHub	Nov 2025 – Feb 2026
- Built a stochastic computing hardware accelerator coupled to a PicoRV32 core via the PCPI coprocessor interface, adding custom instructions (SCGEN/SCDOT/SCACC) that expose the correlation coefficient as a software-visible quantity for edge ML inference. - Verified with Verilator RTL simulation (cycle-accurate counts) and VCD-based switching power analysis on UCI-HAR; manuscript submitted to ICCAD 2026.	
Fuzzy-Controlled Adaptive Cache Management for RISC-V (FuzzyRP + FuzzyStride)	Nov 2025 – Dec 2025
- Embedded a reusable fuzzy inference engine in the L2 cache controller (gem5, RISC-V): FuzzyRP fuses recency and reuse frequency for cache replacement; FuzzyStride throttles hardware prefetcher aggressiveness by real-time accuracy. - Delivered $+10.15\%$ IPC, -47.78% L2 cache misses, and -73.06% memory bandwidth on compiled workloads at $<1\text{KB}$ hardware overhead; accepted for oral presentation at IFIP/IEEE VLSI-SoC 2026.	
Efficient FPGA-Based Parallel Phase Unwrapping Hardware Architecture GitHub	Feb 2026
Designed a low-power, non-iterative DCT-based minimum mean-square phase unwrapping architecture for Digital Holographic Microscopy, with parallel pipelined datapath stages (Laplacian, DCT, frequency processing, IDCT) for fixed, high throughput and low latency.	
Neuromorphic Adaptive-Precision RISC-V Processor (from scratch) <i>Patent filed</i>	Jun 2025 – Jul 2025
Built a complete RISC-V CPU in Verilog (control unit, datapath, ALU, IMEM/DMEM) with a neuromorphic adaptive precision-scaling controller, custom CSRs, and hysteresis/refractory stabilization; prototyped on Xilinx Zynq (Zybo Z7) FPGA with $\sim 12\text{--}17\%$ energy reduction at $<1\%$ performance overhead.	

TECHNICAL SKILLS

Languages: Verilog, SystemVerilog, VHDL, C, C++, Python, RISC-V Assembly, MATLAB, TCL, Bash
Computer Architecture: RISC-V ISA and custom ISA extension design, microarchitecture (pipelining, out-of-order concepts), cache and memory hierarchy, hardware prefetching, branch prediction, vector processing (RVV), performance modeling (IPC, miss rate, bandwidth)
Simulation & Verification: gem5, Spike, QEMU, Verilator, RTL simulation, testbench development, cycle-accurate performance analysis, Linux kernel (RISC-V)
ASIC & FPGA Flow: RTL design, logic synthesis (Yosys, Cadence Genus), place-and-route (Cadence Innovus), Cadence Virtuoso, NC-Verilog, OpenLane, SkyWater Sky130 PDK, RTL-to-GDSII, power/area analysis, Xilinx Vivado, Zynq SoC
Embedded & Protocols: SoC design, embedded systems, SPI, I²C, UART, DMA, edge AI
Other: Git, Docker, CI/CD, Linux, cloud services

PUBLICATIONS

“QIEDP: A Quantum-Inspired Two-Bit Error Correction Protocol for Low-Power Serial Communication in IoT Systems” [Link](#)
• IEEE HiPC 2025 (International Conference on High Performance Computing, Data, and Analytics).
“Neuromorphic Adaptive Precision RISC-V Processor with Real-Time Precision Scaling and Neuronal State Management” [Link](#)
• IEEE HiPCW 2025 (32nd International Conference on High Performance Computing, Data and Analytics Workshops).
“A Two-Bit Error Correction Protocol for Low-Power Serial Communication in IoT Systems” [Link](#)
• VLSID 2026 (39th International Conference on VLSI Design & 25th International Conference on Embedded Systems).
“Interpretable Fuzzy Control for Lightweight Cache Replacement and Prefetch Throttling in RISC-V SoCs”
• Accepted (oral) at IFIP/IEEE VLSI-SoC 2026 (International Conference on Very Large Scale Integration).

PATENTS AND IP

India — Patent (Granted). “Two-Bit Error Detection and Correction in Data Transmission by QIEDP” [Link](#)
• App. No. 202511076945; filed Aug 12, 2025.
India — Patent Application (Published). “Adaptive Dynamic Precision Scaling System for IEEE-754 FPUs”
• App. No. 202511076938; filed Aug 12, 2025.
India — Patent Application. “Bayesian Memory Dependence Prediction and Confidence-Guided Load Scheduling in O3 Processors”
• Filed March 2026.

ACHIEVEMENTS

Samsung Fellowship – Grade I, India Semiconductor Workforce Development Program (ISWDP), IISc Sep 2026
• Selected in the Grade I category from 4,000+ applicants based on academic performance, skills, and institutional ranking.
1st Place, MATLAB/MathWorks Hackathon — BEST Aachen, RWTH Aachen University Jun 2026
Award for Exceptional Excellence in Technical Activities, IIT Mandi May 2026
Top 20 Finalist, YuvaAI 2026 (Indian AI Impact Summit 2026), with ClimMaTech Feb 2026
Global Runner-Up, Google Solution Challenge 2025 Jul 2025
SAPPHIRE Award, Gymkhana, IIT Mandi May 2025