

MRUNAL GAURKAR

[LinkedIn](#) | mrunalgaurkar276@gmail.com | [+91 7666703736](tel:+917666703736) | [GitHub](#)

PROFESSIONAL SUMMARY

B.Tech third-year Microelectronics and VLSI Engineering student at IIT Mandi, with hands-on experience designing and verifying RISC-V processors, custom hardware accelerators, developing RTL, and implementing designs on FPGAs using Verilog along with extending GCC/Binutils for custom instruction sets. Familiar with analog circuit design and CMOS fabrication through coursework. Seeking opportunities to contribute to VLSI and core electronics roles through hardware internships.

EDUCATION

Indian Institute of Technology Mandi

B.Tech, Microelectronics and VLSI Engineering — CGPA: 7.48 (4th sem)

Himachal Pradesh, India

Aug 2024 – Present

Shree Maharishi Vidya Mandir

Class XII — 89%

Maharashtra, India

2024

TECHNICAL SKILLS

Digital Design: RTL Design, Pipelined Processor Architecture, Hazard Detection & Forwarding, FSM, FPGA Design, Timing Analysis, CMOS Logic Design.

Verification & Toolchain: Vivado xsim, Integrated Logic Analyzer (ILA), On-Chip Debugging, GCC & Binutils Internals, Custom ISA Extension Design & Compiler Support.

EDA / Simulation Tools: Vivado (Xilinx), Tanner EDA, MATLAB (Simulink), Altium Designer, SolidWorks.

Programming: Python (Intermediate), Verilog HDL, C (Basics), Machine Learning (Basics).

Core Coursework: Digital & Analog Circuit Design, CMOS Processing, Computer Organization, Control Systems.

Other: Microsoft Office, LaTeX, Arduino, Microchip, GenAI Tools.

PROJECTS

Dual-Core RISC-V SoC with Custom Fixed-Point Accelerator

Ongoing

- Designed the RV32I core pipeline and a custom Q16.16 fixed-point accelerator with 9 custom instructions for a 2-core SoC on a Zynq-7010 FPGA; verified core operation on hardware using Vivado ILA.

Custom RISC-V GCC/Binutils Toolchain

Ongoing

- Extended GCC and Binutils to support the SoC's 9 custom fixed-point instructions as C-callable builtins in the reserved custom-0 opcode space; verified code generation from C source through assembly, linking, and disassembly.

RV32I Branch Delay Slot Emulation — On-Silicon FPGA Deployment

May 2026

- Modified pipeline control to implement MIPS-style branch delay slots and developed a Python instruction scheduler to fill them; achieved a 60% fill rate and reduced CPI from 2.615 to 1.888 on a Zybo FPGA at 114.67 MHz, verified using Vivado xsim and ILA.

Pipelined RV32I RISC-V Processor with MAC Accelerator

March 2026

- Designed and verified a 5-stage RV32I pipeline in Verilog with partial branch-flush control; integrated a tightly coupled custom Multiply-Accumulate (MAC) unit, synthesizing at 100 MHz on a Xilinx Artix-7 FPGA (940 LUTs, 6 DSP48E1 slices).

Analog Circuit Design & CMOS Fabrication Coursework

Jan – May 2026

- Completed coursework in analog circuit design (amplifiers, filters, biasing) and hands-on CMOS processing experiments, gaining exposure to cleanroom protocols and semiconductor fabrication workflow.

Additional Projects

- Soil Image Classification** — Developed a 7-class soil classification pipeline using color, LBP, and HOG features with an SVM, Random Forest, and XGBoost ensemble; achieved 82.63% validation accuracy and 0.81 weighted F1-score.
- Obstacle Avoidance Robot** — Developed an obstacle avoidance robot with sensor-based feedback for navigation along curved paths with surrounding obstacles.
- Control Systems Modeling (MATLAB/Simulink)** — Controller design for physical systems, simulation-to-hardware experimentation.
- Tabletop Filament Extruder** — Electrical architecture for a low-cost extruder converting waste PET into 3D-printing filament.

COMPETITIONS & CERTIFICATIONS

- Introduction to the Internet of Things and Embedded Systems (Coursera) — UC Irvine Aug 2026
- KrackHack (IIT Mandi) — Front-end development for a team-based web project May 2025
- RoboWar (Utkarsh, Tech fest) — Collaborated in the design of an RC robot. Sep 2024