

Priyanshi Malviya

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OVERVIEW

Focused VLSI graduate with a strong foundation in digital circuit design and memory architecture. Highly proficient in RTL design using Verilog, with hands-on experience developing 4-bit adder/subtractor circuits, 4-bit comparators, and static RAM (SRAM) during my M.Tech. Adept at utilizing EDA tools including Cadence Virtuoso and MATLAB, backed by a deep understanding of device-level semiconductor physics from research at IIT Gandhinagar. Aiming to leverage my expertise in digital logic, circuit optimization, and analytical problem-solving in a high-impact digital design role.

RELEVANT COURSES

Digital VLSI circuit design, Memory devices, Architectural design of digital integrated circuits, System design lab, Physics of transistors, CMOS analog IC design, Semiconductor materials and fabrication processes, Advanced semiconductor devices, Microelectronics lab, Analog IC design lab.

INTERNSHIP / TRAINING / EXPERIENCE

Junior Research Fellow (JRF)

Aug 2025 – Present

IIT Gandhinagar

- **Project:** Universal Multi-domain On-Chip ESD Protection Design for Neurostimulators (TSMC 65nm Technology).
- Executing the architecture, multi-domain parametric transient simulation, and robust physical layout verification loops of electrostatic discharge (ESD) protection grids designed for sensitive biomedical chip interfaces.

Project Intern

May 2024 – July 2024

IIT Indore

- **Framework:** National Chips to Startup (C2S) Project NSDCS Laboratory.
- Designed and laid out a high density 6T SRAM array and peripheral blocks using Cadence Virtuoso.
- Validated read/write stability via extensive SNM and transient evaluations, and verified in-memory computing topologies for logic execution.

Teaching Assistant

IIT Gandhinagar

- Coordinated the semiconductor devices course for 120 B.Tech students which included taking tutorials, quizzes, and use of nanoHUB software.

EDUCATION

Indian Institute of Technology (IIT), Gandhinagar	JRF	2025 – 2026
Indian Institute of Information Technology (IIIT), Guwahati	M.Tech	2023 – 2025
Madhav Institute of Technology and Science, Gwalior	B.Tech	2019 – 2023
Rashtriya Vidhya Mandir	12th	2018 – 2019
Advanced Academy	10th	2015 – 2016

PROJECTS

TCAD Process and Device Simulation of MOS device

- Executed comprehensive 2D/3D process and device level simulations of CMOS to model physical profiles and extract the current vs voltage and capacitance vs voltage measurements, alongside mixed-mode TCAD analysis to evaluate the transient responses and DC transfer characteristics of CMOS logic configurations.

FinFET Process and Device Characterization

- Executed comprehensive process and device simulation for a FinFET architecture, incorporating advanced mobility and quantum confinement models.
- Benchmarked key electrical parameters such as ON/OFF currents and subthreshold swing and analysed 3D electron density profiles against planar MOS equivalents.

p-Gate GaN HEMT Electrostatics

- Investigated the structural and electrostatic properties of a p-Gate GaN HEMT, focusing on 2DEG concentration and band diagram interpretations.
- Analyzed device performance and breakdown trends by varying barrier thickness and gate-to-drain lengths to optimize electric field distribution.

Low Power SRAM-Based CAM for Networking Applications | IIIT Guwahati (90nm Node)

- Architected a custom low-voltage Content Addressable Memory (CAM) layout optimized for hardware networking routing table search speed upgrades.

- Integrated optimized match-line sense amplifiers and customized low-power dynamic peripheral circuitry to maximize operating power margins.
Design and Implementation of a 4x4 SRAM Array | IIT Indore (180nm Node)
- Independently carried out schematic design, full physical floorplanning, routing, and clean GDS-II export of a 4x4 custom memory block in the NSDCS Lab.

TECHNICAL SKILLS

- **Languages:** Verilog, C
- **EDA Tools:** Cadence Virtuoso, Xilinx Vivado, Synopsys Design Compiler TCAD, MATLAB, Simulink
- **Technical:** verilog, SRAM array design, SRAM based CAM design, Diodes, MOSFET, Advanced semiconductor devices: FinFET, Gate all around nanosheet and nanowires FET, HEMT, semiconductor devices, digital circuits, CMOS circuits, ASIC design flow, Static timing analysis, clock domain crossing(CDC), and synthesis and simulation

CERTIFICATIONS & ACHIEVEMENTS

- **Junior Research Fellowship (JRF):** Awarded competitive institutional research position at IIT Gandhinagar (2025).
- **MATLAB Stateflow Onramp:** Technical competency certification issued via MathWorks (October 2023).
- **C2S Project Certification:** Earned formal institutional recognition for core milestone layout deliveries from IIT Indore (2024).
- **Indo-South Korea Conference:** Selected Event Management Team organizer for the international bilateral scientific summit.